PWB Dielectric Substrates for Lead-Free Electronics Manufacturing

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Abstract
In order to safely accommodate the increased thermal and mechanical requirements of lead-free assembly technology, extensive testing of the printed wiring board (PWB) substrate is required to confirm that there are no compromises in performance and long term reliability when moving away from lead. This paper presents a comparison of four (4) different commercially available PWB substrate materials, including one produced specifically to handle lead-free soldering, using both traditional thermal shock testing and accelerated thermal cycling. The use of the Interconnect Stress Test (IST) was chosen for the accelerated life cycle test. A generic 22 layer PWB test vehicle was subjected to various pre-conditioning environments in order to simulate the stress generated during both lead-containing and lead-free assembly. These test vehicles were then cycled to failure. Using this test methodology, this paper will allow the reader to obtain a comparison, under lead-free assembly test conditions, of the traditional thermal robustness tests with the IST thermal cycling test. It will also provide an indication of the impact on the PWB of moving from a lead-containing assembly environment to one that is lead-free.

Introduction
Despite the relatively low consumption of lead by the electronics industry[1], there is currently a strong drive globally to replace the use of lead. This drive seems to be primarily related to both legislative initiatives[2] and marketing efforts by electronics OEM's. The most significant legislative pressure comes from the Japanese electronics recycling directives and the RoHS (Restriction of Hazardous Substances) and WEEE (Waste from Electrical and Electronic Equipment) initiatives in Europe.

In order to facilitate the conversion to a lead-free environment the equipment, materials, and processes used to fabricate lead free assemblies must be extensively studied to insure that the elimination of lead will not jeopardize the performance and long term reliability of the resulting lead free electronic systems[3]. A key component used in all electronic systems is the printed wiring board (PWB). In order to fully understand the ramifications of moving to a lead-free electronic system, a significant amount of study is required to determine the proper selection of PWB dielectric substrate materials that will withstand the significant increase in thermal stress caused by this conversion. Previous work[4,5] has suggested that standard FR-4 substrate materials with Tg ratings of 130-140^{o}C (DSC) have difficulty withstanding the thermal stress of lead-free assembly, even in relatively low layer count PWB designs. It is, therefore, imperative that the electronic design and manufacturing community understand the proper selection of PWB substrate materials that will assure performance and reliability in lead-free assemblies.

Background
For component assembly onto bare printed wiring boards, the electronics industry appears to be moving forward with the specification of Sn/Ag/Cu (SAC) alloys for lead-free processing[6]. Figure 1 illustrates the approximate reflow temperature requirements of these SAC alloys compared to eutectic Sn/Pb.

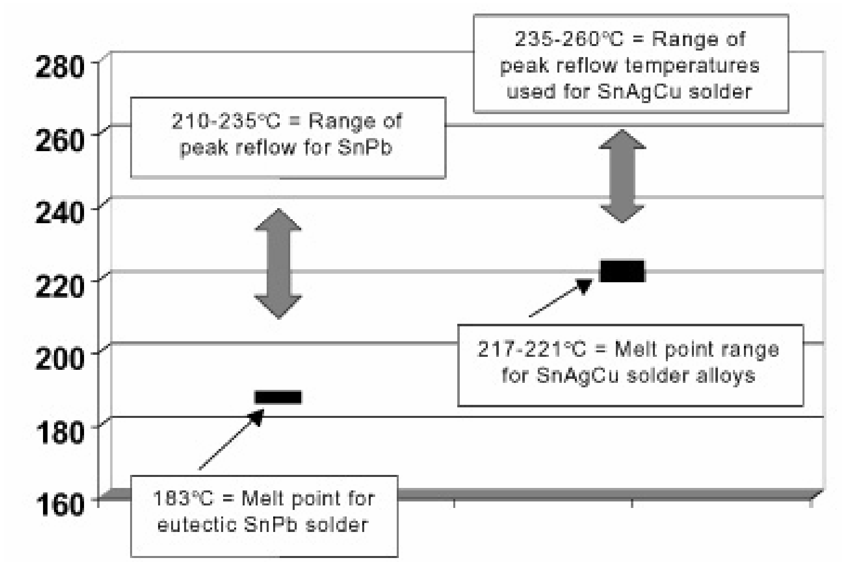


Figure 1[6] – Sn/Pb and Sn/Ag/Cu (SAC) Alloy Reflow Temperatures

The liquidus temperature of SAC alloys is in the range of 217-221°C, compared to 183°C for eutectic Sn/Pb solder. Depending on the thermal loading / complexity of the assembly, the profiling accuracy of the oven, and the alloy chosen, the peak reflow temperature for SAC alloys is estimated to be 235-260°C. In addition, the absence of a sharp eutectic transition with SAC alloys results in a "pasty range" for the alloy and requires, in some instances, that the time above liquidus be extended by 15-30 sec. The result of this transition from eutectic solder to an SAC alloy, therefore, requires a peak temperature increase of up to 40°C and a time above 220°C that is considerably longer than that currently encountered. This combination of requirements puts substantial additional thermal stress on all exposed materials, including the PWB.

This study will focus on the effect of this increased thermal stress on a relatively high layer count PWB and will seek to determine whether the substrate materials tested are capable of withstanding this stress without reliability issues.

Material Selection

For this study, four PWB substrate materials were chosen. Two of the materials were high Tg (Tg>170°C) FR-4 epoxy resins, one was a mid-Tg (Tg=155°C) FR-4 epoxy system, and one a high Tg (Tg=210°C) enhanced epoxy resin formulation. All Tg's reported here were measured by DSC, unless otherwise noted. Based on the results of previous testing with low Tg FR-4 substrates[7,8] in a lead free assembly environment, it was determined that low Tg FR-4 materials (Tg=130-140°C) would stand little chance of performing adequately in this test, given the layer count and resin content of the test vehicle. It was, therefore, decided that a range of materials with varying Tg's, beginning at 155°C, should allow for the discrimination of their capability to perform adequately in this test matrix. Table 1 provides a summary of select attributes of each of the PWB substrate materials. All test materials were supplied by Park / Nelco.

Test Vehicle Design

For the IST test matrix, a generic 22 layer PTH/Post interconnect test vehicle was designed with the assistance of PWB Interconnect Solutions Inc[9]. This vehicle had four independent daisy chain circuits which were finished with either 0.040", 0.015", or 0.040" and 0.015" drilled via diameters on a 0.040" or 0.080"grid. The test vehicles were laminated to a thickness of 0.120". All inner layer construction was 2116 E-glass reinforced with a nominal resin content of 53%. All copper foil used was 35 um, with the exception of Material B, which was built using 18 um Cu inner layers. Aspect ratios were 3:1 for the 40 mil vias and 8:1 for the 15 mil vias.

This test vehicle design was specifically chosen to represent a range of current high technology PWB substrates in production globally. This design might represent a typical daughter card

Material Type/Property	Material A	Material B	Material C	Material D
Resin System	High Tg Epoxy	Enhanced High Tg	High Tg Epoxy	Mid Tg Epoxy
Primary Cure Chemistry	Non-Dicy	Non-Dicy	Dicy	Dicy
Tg (DSC)	175°C	210° C	175°C.	155°C.
CAF Resistant	Yes	Yes	No	Yes
Contains Bromine	Yes	Yes	Yes	Yes
Dielectric Constant (1 MHz)	4.3	3.9	4.3	4.5
Dissipation Factor (1MHz)	0.020	0.009	0.023	0.018
X/Y axis CTE (-40 to +125°C)	12-14 ppm/°C	10-14 ppm/°C	12-16 ppm/°C	12-15 ppm/°C
Low Z-CTE Resin Chemistry	Yes	Yes	No	Yes

Table 1 – PWB Substrate Material Properties

PWB used in storage area networks, internet routers and switches, or semiconductor test equipment. The relatively high resin content of the construction was chosen to provide a severe challenge during assembly due to the increased z- axis expansion of the epoxy resins under lead-free assembly conditions.

PWB Fabrication

A total of thirty test vehicles of each material type were fabricated by Speedy Circuits, Huntington Beach, CA for IST testing. All panels were processed in an 18”x24” format at the same manufacturing facility during approximately the same time frame. Panels were metallized with conventional electroless copper and electrolytic copper without pulse rectification. Desired nominal total Cu thickness was 0.001” minimum. The surface finish for all panels was Sn/Pb (HASL). A HASL finish was chosen to subject the test vehicles to an additional thermal excursion before any simulated assembly pre-conditioning. No special precautions were taken by the fabricator and the panels were routed and drop shipped directly to the test site.

Thermal Reliability Testing

Two types of thermal testing were performed on each material set. The first set of tests may be termed “traditional” PWB substrate material tests that are widely recognized in the industy but are, in some cases, not standardized from vendor to vendor. The second set of tests involved IST testing using a series of progressively more stringent pre-conditioning environments.

For the traditional thermal testing (TMA, T_{260}, T_{288}, Solder Floats, etc.), an 8 ply, 7628 based test vehicle was used for all materials. Test conditions and procedures were standardized and identical for all substrate types. Nominal resin content of the test vehicle was 44%. All testing was performed at the Park / Nelco Research and Development laboratories in Anaheim, CA.

All IST testing was performed at PWB Interconnect Solutions, Inc. in Ottawa, Ontario, Canada. Test vehicle pre-conditioning for the NEMI lead free profiles was performed at Celestica in Toronto, Canada. Table 2 provides detail on the number of test vehicles subjected to each type of pre-conditioning step. A greater sample size would have been preferred for each of the test conditions; however, financial realities lead to a determination of the minimum number of samples required to obtain valid data. Prior to pre-conditioning, all coupons were subjected to electrical pre-screening to determine bulk resistivity for each material type used.

During pre-screening, it was discovered that Material B samples exhibited resistance values that were approximately double those of the other material types. This confirmed that the construction of Material B test vehicles used 18 um Cu rather than the 35 um used for the other test materials. Graph 1 highlights these results.

The dashed red line in Graph 1 displays the Material B resistance values with a correction factor applied to compensate for the 18 um Cu foil. This graph further indicates that Material D had the thinnest plated Cu deposit while Material C had the thickest electroplated Cu. The mean Cu plating thickness inside vias on the vast majority of the coupons did not meet the intended minimum of 0.001”. The electrical pre-

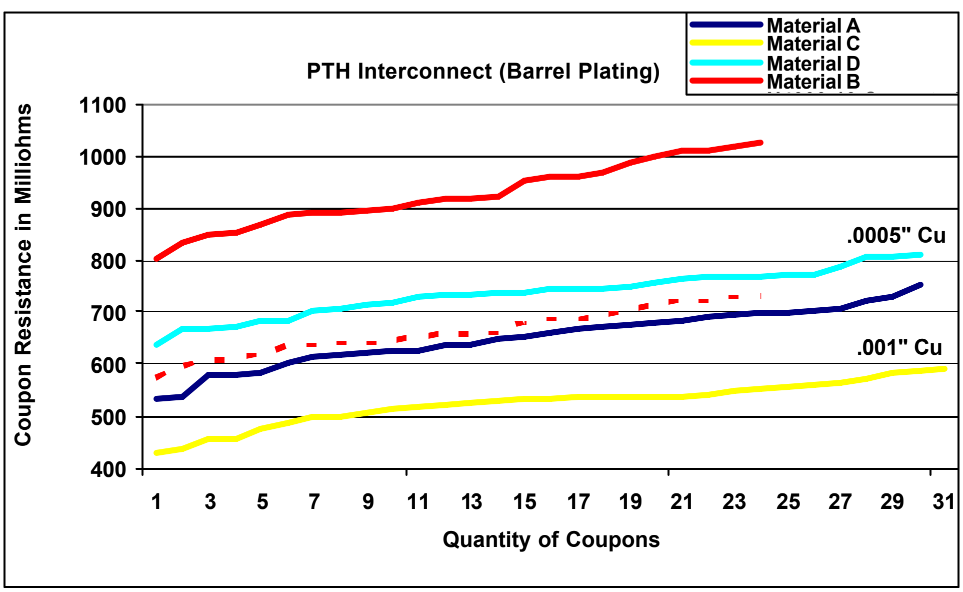
Coupon Design	Test Condition	Material A	Material B	Material C	Material D
0.015" vias / 0.040" Grid	As Received	9	9	9	9
0.015" vias / 0.040" Grid	3x at 220°C	3	3	3	3
0.015"+0.040" vias /0.080" Grid	As Received	3	3	3	3
0.015"+0.040" vias /0.080" Grid	3x at 220°C	3	3	3	3
0.015" vias / 0.040" Grid	3x at 255°C	6	6	6	6
0.015" vias / 0.040" Grid	3x @ NEMI SMT	6	6	6	6

Table 2 – Number of Test Vehicles Subjected to Pre-Conditioning

screening estimated the test coupons to have an average of 0.0008" of electrolytic copper plating in the PTH. Microsections confirmed the estimated copper thickness. Several coupons for Material B measured 0.0004"-0.0005" of copper in the central zone of the barrel. Coupons associated with Material C measured the thickest copper, with an average copper ranging between 0.0008" and 0.0009".

After pre-screening, the test vehicles were subjected to pre-conditioning as per the test conditions described in Table 2. All pre-conditioning was accomplished via the IST test equipment with the exception of the 3x NEMI SMT profiles. For this test condition, the test coupons were physically run through an SMT assembly reflow oven under the temperature profile outlined by NEMI for lead free surface mount assembly. The peak reflow temperature of this profile was 255°C.

After pre-conditioning, all test vehicles were subjected to IST testing. All IST testing was performed by PWB Interconnect Solutions, Inc. The IST test heats the vehicle by applying a direct current to a serpentine daisy chain test pattern in the multilayer coupon. The coupon is heated to 150°C for 3 minutes, allowed to cool to ambient temperature for 2 minutes (cooling is accomplished using a motorized fan blowing ambient air under the coupon), and re-heated to 150°C. This sequence comprises one IST cycle. Coupons are tested to failure or to some pre-determined number of cycles. The cut off point chosen for this test was 1000 cycles. A coupon failure is recorded if the network resistance within the coupon rises more than 10% from its initial value.



Graph 1 – Test Coupon Resistance and Corresponding Copper Thickness

Discussion of Test Results

When examining the performance of PWB substrate materials in a lead-free assembly environment, there are several traditional metrics that may be used to judge each material. Among these are the Tg of the product, the decomposition temperature, the time to delamination at 260°C or 288°C, the z-axis expansion characteristics, and the solder float test. Given the relative complexity of the lead-free test vehicle used for this study and the high resin content of the build, one would expect that a material with a high Tg, high TGA, low z-axis expansion, and good performance in the delamination tests would be the most suitable material for the lead-free assembly environment.

A comparison of these traditional material properties for the four test substrates is given in Table 3. The two most robust substrates in this test matrix were Material A and Material B, with Material B exhibiting the longest T_{260} and T_{288} times and the highest Tg values. Material B also had the best performance in the solder float test. Material C had the lowest T_{288} duration and exhibited a relatively high z-axis expansion rate, particularly when measuring out to 288°C. Based on these traditional tests, one could argue that the order of suitability for environments requiring a high thermal tolerance such as lead-free assembly would be B, A, D, and C.

Property/Condition	Material A	Material B	Material C	Material D
Resin System	High Tg Epoxy	High Tg Enhanced	High Tg Epoxy	Mid Tg Epoxy
Tg (DSC)	175°C	210° C	175°C.	155°C.
Tg (TMA)	165°C	200° C	170°C.	150°C.
Tg (DMA)	195°C	240°C	180°C	160°C.
Degradation Temperature (TGA - 5% weight loss)	362°C	357°C	325°C	330°C.
Z axis expansion* (50 to 260°C in %)	3.20%	3.50%	3.70%	3.80%
Z axis expansion (50 to 288°C)	4.20%	4.10%	5.90%	4.60%
Moisture Resistance (24 hr. immersion)	0.15%	0.10%	0.15%	0.07%
T260	30 min.	> 30 min.	7 min.	16 min.
T288	6 min.	9 min.	N/A	1.4 min.
Solder Float (4"x4" Cu Clad) (288°C. - time to failure)	550 sec.	>600 sec.	230 sec.	263 sec.

Table 3 – Thermal Test Data of Substrate Materials

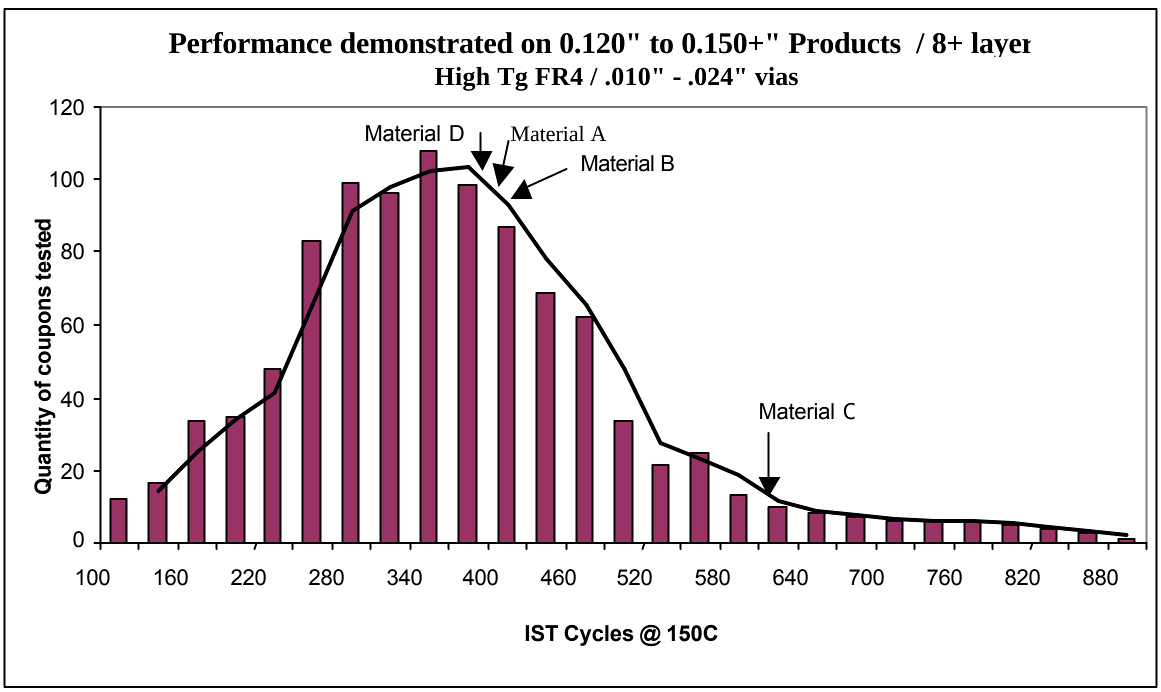
The summarized results of the IST testing of all coupons are presented in tabular form in Table 4. These results showed that all coupons demonstrated the plated through vias (PTV) to be the dominant failure mechanism. This was caused by the late onset of fatigue causing barrel cracking in the central zone of the PTV[10]. This fatigue barrel cracking is the expected and desired failure mode for a plated through via during thermal cycling[11]. Furthermore, no coupons measured resistance degradation in the inner layer to PTH barrel (post) interface. In both the as received state and for all pre-conditioning environments, all the substrate materials demonstrated a relatively high level of capability, taking into account the complexity of the test vehicle design. Graph 2 presents the as received IST data as a comparison to a statistical database of high Tg FR-4 materials with 8+ layers and a thickness of 0.120" to 0.150+". Material A, C, and D exhibited very little, if any, degradation in performance when comparing the as received test coupons to the two lead-free assembly simulations.

When examining the IST test data, there were quite a few unexpected aspects of the results. The substrate material with the highest level of capability in traditional thermal testing, Material

Table 4 – Summarized Results of IST Testing Under Various Pre-conditioning Environments

Coupon Design	Test Condition	Material A	Material B	Material C	Material D	All
.015” vias / .040” grid	As Received	390	415	615	374	448
.015” vias / .040” grid	3X @220C	500	420	485	408	453
.040”+.015” /.080” grid	As Received	360	357	764	365	462
.040”+.015” /.080” grid	3X @220C	357	349	626	561	473
.015” vias / .040” grid	3X @255C	440	193	574	374	390
.015” vias / .040” grid	3X NEMI SMT	580	322	647	401	477

B, survived 322 cycles under the NEMI lead-free pre-conditioning test, compared to 647 cycles for Material C. Under all test conditions except the 3x @ 220^{o}C pre-conditioning, Material C demonstrated the highest IST cycle counts. In an attempt to understand and explain these unusual results, the copper plating thickness of all materials were again examined. Table 5 provides additional Cu plating thickness data for both the 3x @ 255^{o}C and the NEMI SMT pre-conditioning environments for all four material types. When reviewing this information in conjunction with the IST test results, the influence of electroplated Cu thickness on the performance of any PWB substrate by IST testing becomes abundantly clear. It is reasonably certain that Material C benefited from a Cu deposit that was much closer to the desired 0.001” minimum. At the other extreme, Material B, a material known for its robust thermal resistance in many high layer count production applications, displayed lower IST cycle counts in this testing. One aspect of this performance can be related to plated Cu thickness. Another aspect may have been the 18 um Cu inner layers in the test vehicle construction for Material C. In a previously cited study, the author states ‘with the higher temperature reflow profiles expected with lead-free assembly, 1/2 ounce copper significantly degrades reliability’[12]. In all cases, it appears that the copper plating reduced the ability to differentiate between materials and certainly dominated the overall results.



Graph 2 – IST Performance of Substrate Materials in Relation to Historical IST Data

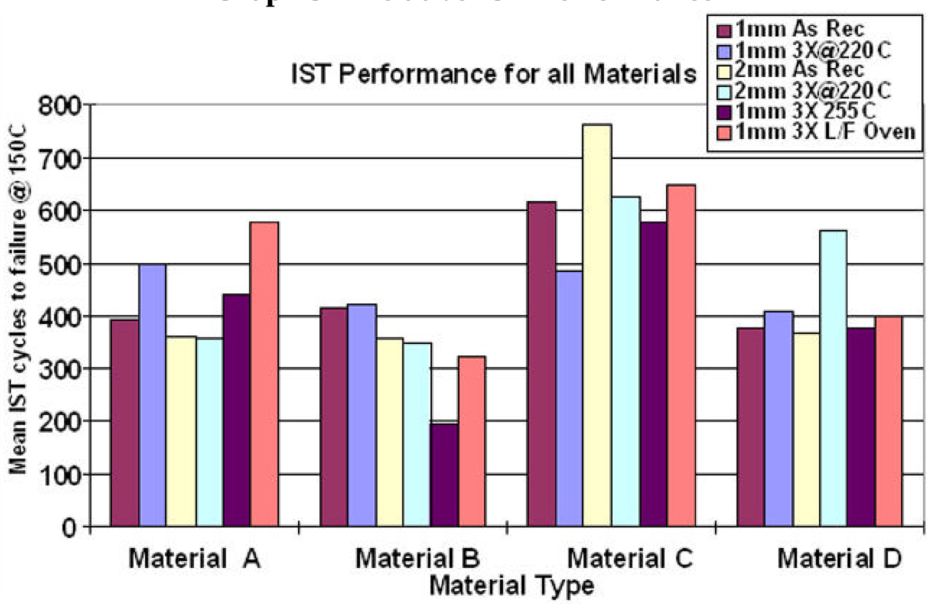
Table 5 – Microsection Cu Thickness Data for Lead-Free Assembly Test Vehicle

Material / Test	Material A	Material B	Material C	Material D
3x @ 255°C				
Top	0.0019”	0.0013”	0.0021”	0.0018”
Mean Barrel	0.0006”	0.0007”	0.0009”	0.0006”
Min. in Barrel	0.0004”	0.0006”	0.0007”	0.0004”
Bottom	0.0019”	0.0013”	0.0021”	0.0017”
NEMI SMT				
Top	0.0019”	0.0013”	0.0022”	0.0018”
Mean Barrel	0.0007”	0.0007”	0.0009”	0.0005”
Min. in Barrel	0.0005”	0.0006”	0.0006”	0.0004”
Bottom	0.0019”	0.0013”	0.0021”	0.0019”

Conclusions

In spite of the relatively low Cu electroplating thickness encountered in this study, the overall performance of all substrate materials in IST testing was very solid. Graph 3 provides a graphical representation of the each material’s performance in each of the IST tests. The lack of degradation in the IST test results as a result of the progressively more severe preconditioning performance in any type of test condition. This study has shown that the effect of Cu plating thickness and integrity on the results of IST testing are quite significant. It is, therefore, vital that any tests run to compare PWB substrate materials be performed with identical Cu plating processes and with all plating performed under identical process conditions. The effect of Cu

Graph 3 – Relative IST Performance



steps represents that all four of the substrates tested should perform adequately in lead-free reflow conditions requiring 3 or fewer thermal excursions with high layer count, high resin content PWB constructions. In addition, a cautionary note is in order for the use of IST testing to compare PWB substrate material plating can be further illustrated by comparing the performance, in Graph 3, of Material A with Material C. Material C appears to be more robust but that is due to the higher amount of copper plating in the through hole. This graph illustrates that Material A degrades less and, in some instances, improves after thermal shock whereas Material C degrades in each instance.

A full statistical treatment of the IST data is not warranted in this report due to the small sample size used for some of the tests in the study. Also, a detailed examination of the cross sections of each of the materials tested would be too lengthy to address here. Further information can be supplied by the authors upon request. The authors wish to thank PWB Interconnect Solutions, Inc. for their assistance with the test design and for their testing services and Speedy Circuits for the test vehicle fabrication.

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